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AMENDMENTS TO THE CLAIMS

Claims 1-12 (Canceled)

13. (currently amended) A system of cascaded devices, comprising:

a first device having a first input for receiving a request signal from a first source, a second input for receiving a first reply signal from said first source, a first output for outputting said request signal, and a second output for outputting a second reply signal;

a first buffer having a first programmable buffer stage depth comprising a first number of buffer stages, the first buffer ~~and~~ being coupled to said first device for receiving said outputted request signal; and

a second buffer having a second programmable buffer stage depth comprising a second number of buffer stages, the second buffer ~~and~~ being coupled to said first device for receiving said second reply signal.

14. (Previously presented) The system of claim 13, further comprising an output bus, said output bus being coupled to said first and second buffers and to a second device.

15. (Original) The system of claim 13, wherein said second reply signal is generated from said request signal and said first reply signal.

16. (Original) The system of claim 14, wherein said first buffer buffers said outputted request signal when said second device has a lower latency than said first device.

17. (Original) The system of claim 14, wherein said second buffer buffers said second reply signal when said second device has a higher latency than said first device.

Claims 18-19 (Canceled)

20. (Previously presented) The system of claim 19, wherein buffer stages in said first buffer and said second buffer are bypassed.

21. (Original) The system of claim 14, wherein said first device and said second device are content addressable memory (CAM) devices.

22. (Previously presented) The system of claim 13, wherein said first and second buffers are part of a same buffer unit.

Claims 23-62 (Canceled)

63. (new) The system of claim 13, wherein the first programmable buffer stage depth is different than the second programmable buffer stage depth.

64. (new) The system of claim 13, wherein the first programmable buffer stage depth is the same as the second programmable buffer stage depth.